Reference numbers

1	Clock receiver circuit device
2	Circuit
3a	Clock connection
3b	Clock connection
4	Transfer gate
5	Transfer gate
6	Transfer gate
7	Transfer gate
8a	Line
8b	Line
8c	Line
8d	Line
8d'	Line
8d''	Line
8e	Line
9a	Line
9b	Line
9c	Line
9d	Line
9d'	Line
9d''	Line
9e	Line
10a	Line
10b	Line
11a	Output line
11b	Output line
11c	Input
11d	Input
12	Line
13	Line
14	Line
15	Line
104a	Transistor
104b	Transistor
105a	Transistor

105b	Transistor
107a	Line
107b	Line
110	Line
115a	Line
115b	Line
115c	Line
116	Current source
117	Line

FIG 1

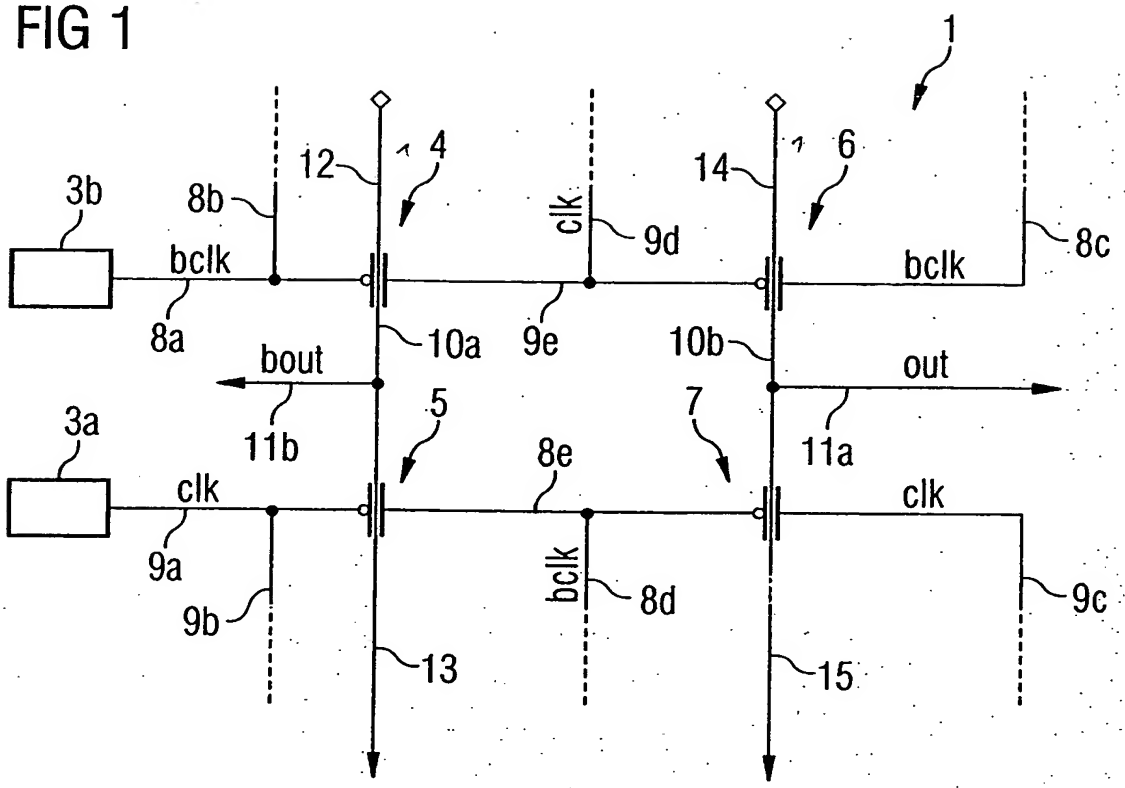
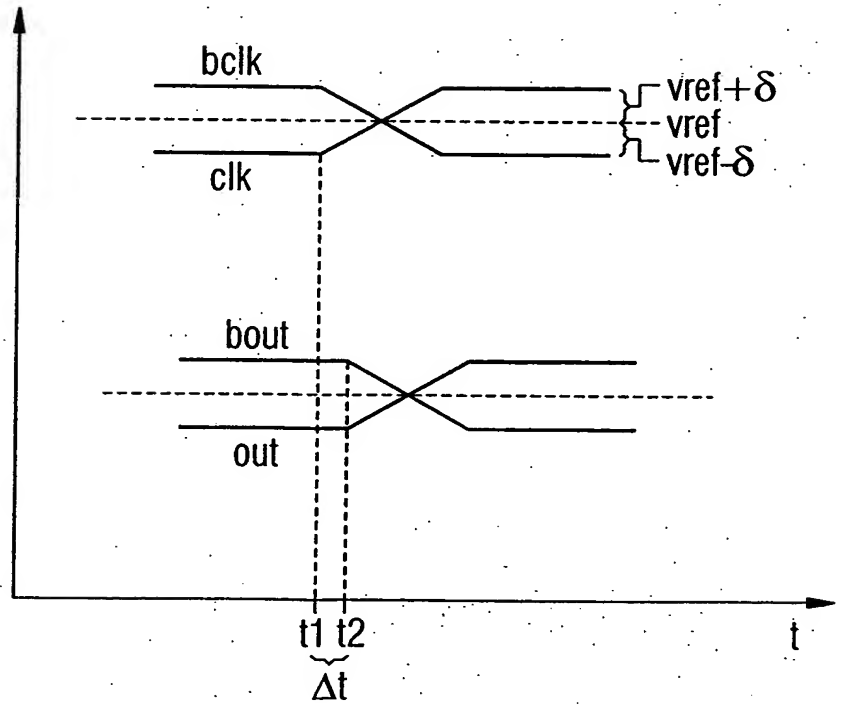

1
3b
8b
12
4
14
6
clk
9d
8c
bclk
bclk
8a
10a
9e
10b
bout
out
3a
11b
5
7
11a
8e
clk
clk
9a
bclk
8d
9c
9b
13
15

FIG 2


bclk
vref+δ
vref
vref-δ
clk
bout
out
t1
t2
t
Δt

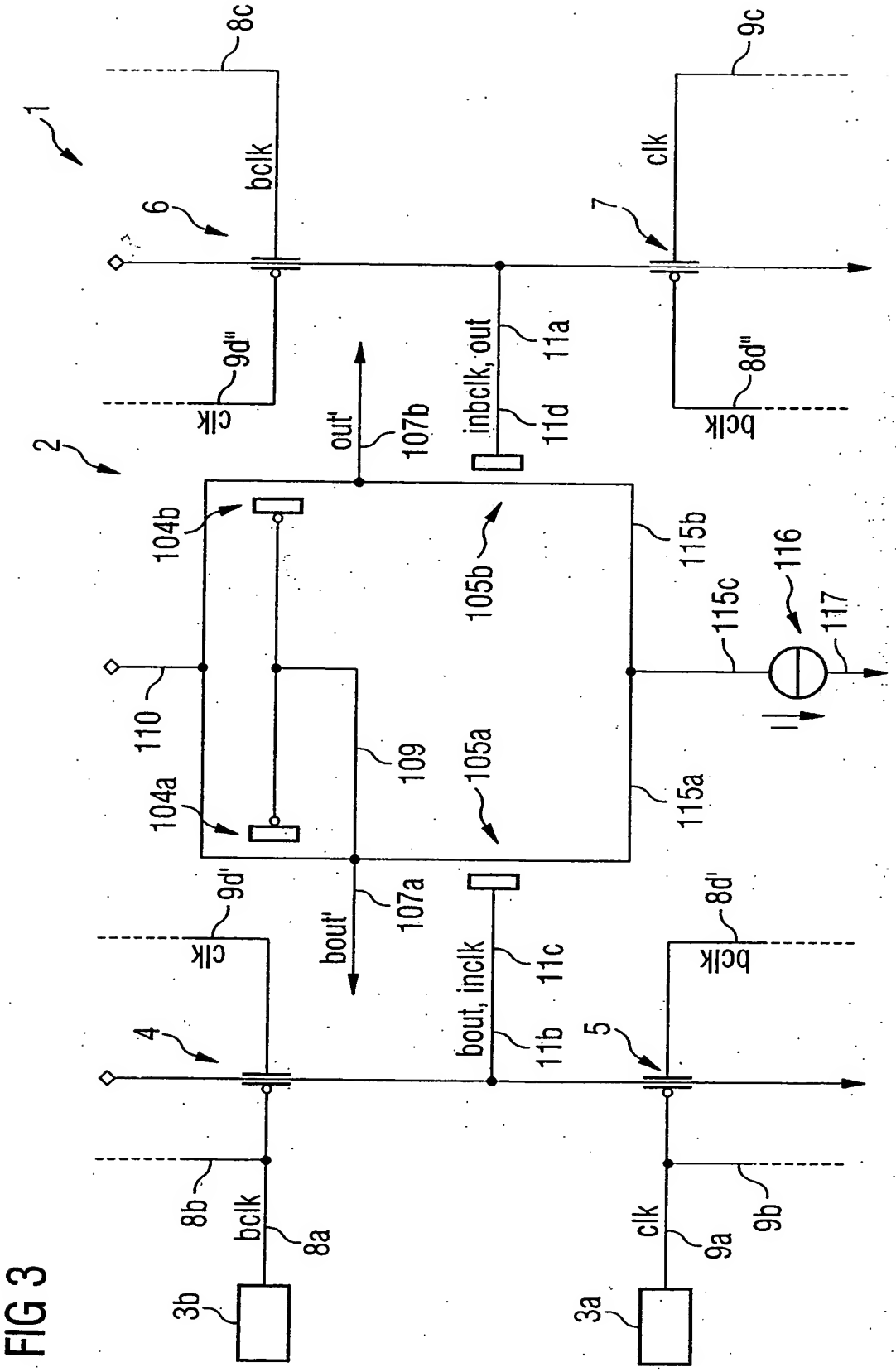

1
2
3a
3b
4
5
6
7
8a
8b
8c
8d'
8d''
9a
9b
9c
9d'
9d''
104a
104b
105a
105b
107a
107b
109
110
11a
11b
11c
11d
115a
115b
115c
116
117
I
bclk
clk
bclk
clk
bout, inclk
bout'
inbclk, out
out'
clk
bclk
clk
bclk

FIG 3